Enhanced 130 nm Generation Logic Technology Featuring 60 nm Transistors Optimized for High Performance and Low Power at 0.7 - 1.4 V

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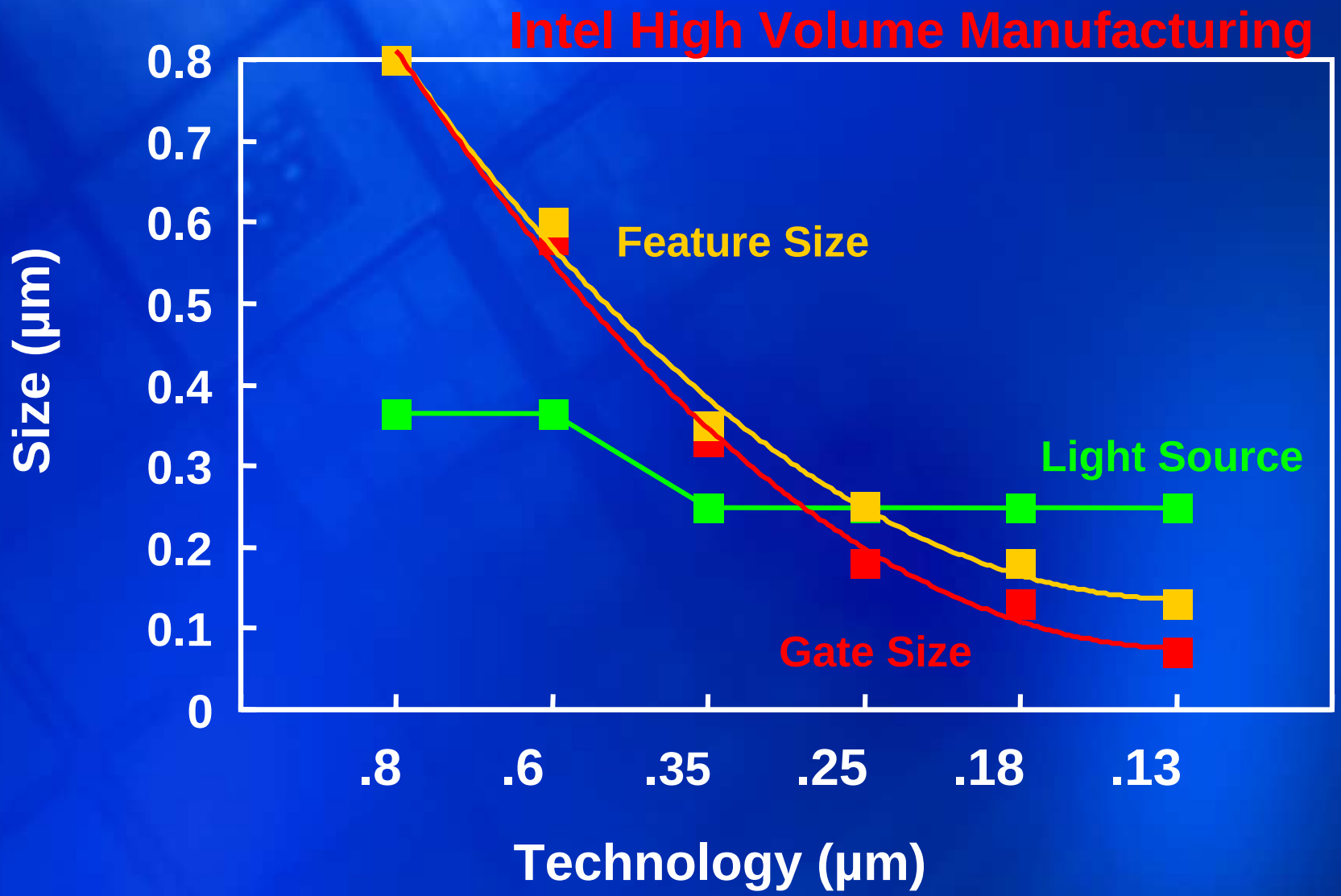
Outline

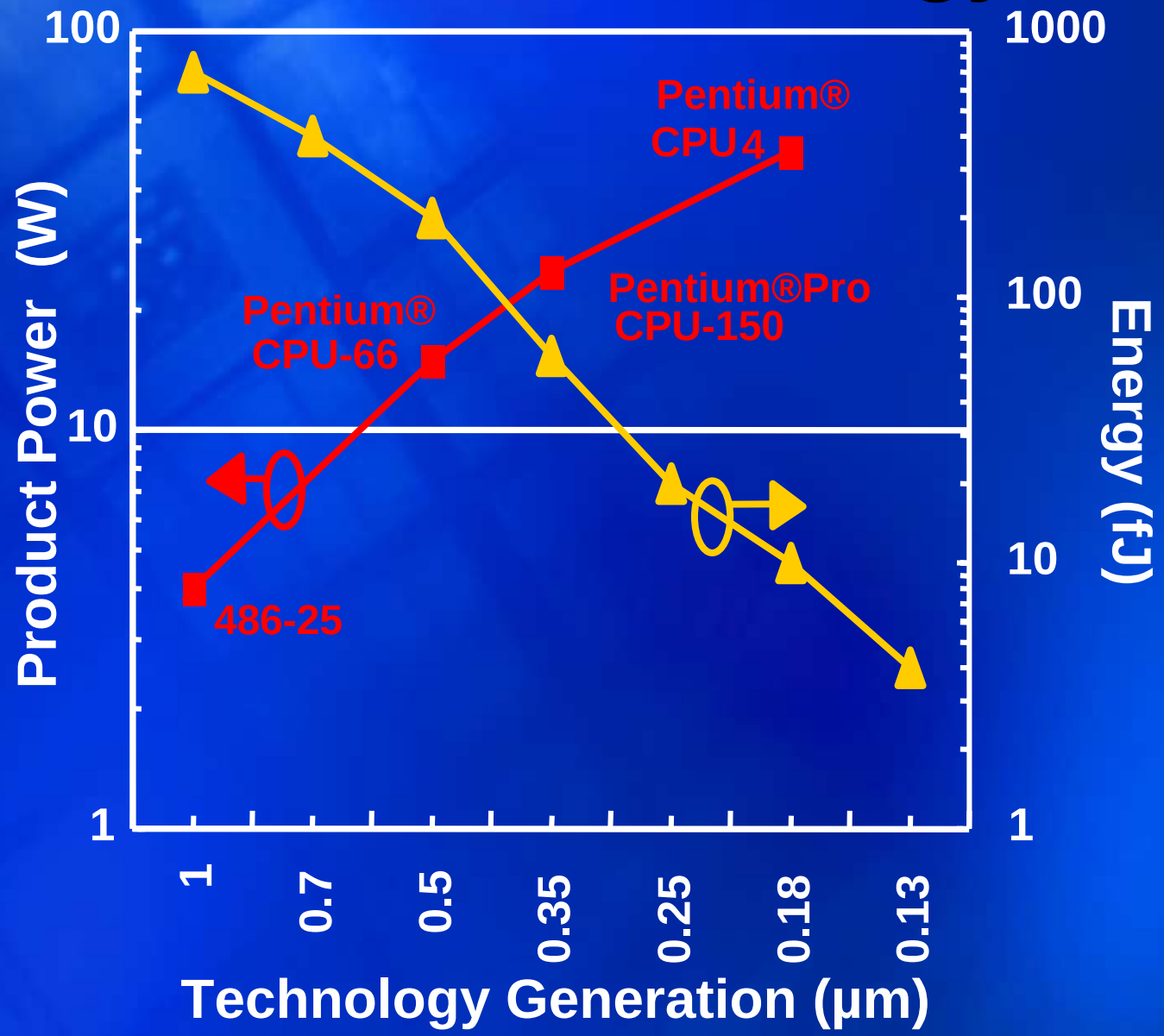
- Introduction
- Process Flow and Technology Features
- Enhanced Transistor Features
  - 1.5 nm T_{ox} with improved oxide TTF
  - 60 nm transistors
  - Low DIBL
  - Process changes to support 0.7 to 1.4 V operation
- Product Performance
- Conclusions

Transistor Gate Scaling Trend



- Gate CD in production ~60 nm for 130 nm node

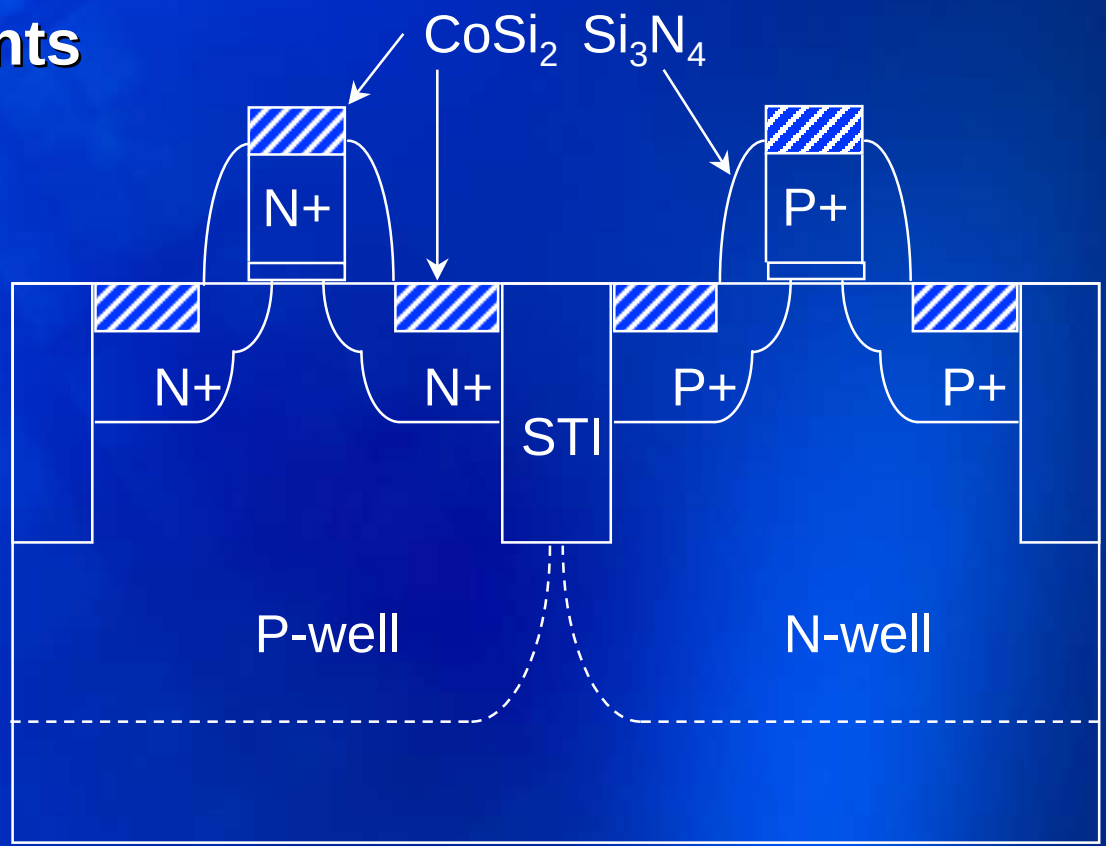
Product Power and Energy Trends



- Voltage scaling needed to control power

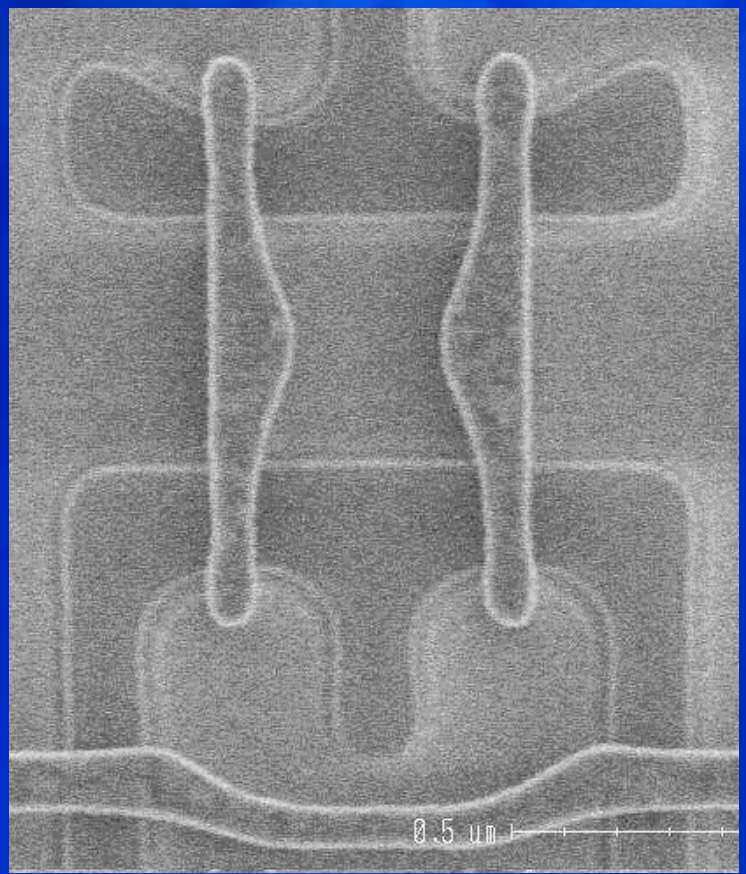
Front End Process Flow and Features

- Shallow Trench Isolation
- Well & V_T Adjust Implants
- Gate Oxide Formation
- Poly Gate Patterning
- Shallow Source Drain Extensions
- Halo Implants
- Si_3N_4 Spacer
- Deep Source/Drain
- Co Salicide

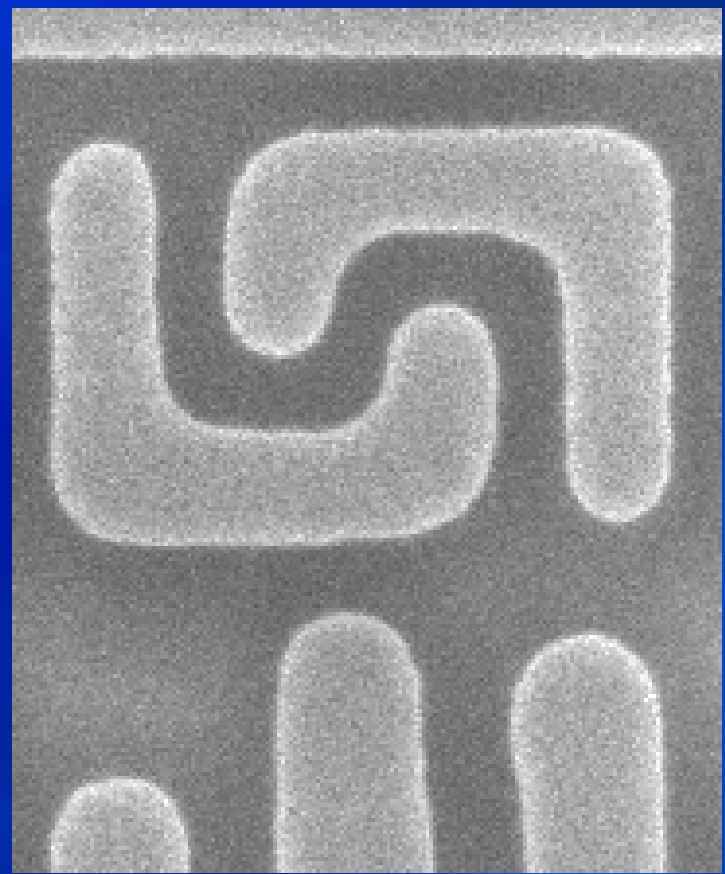


2.0um² 6-T SRAM Cell

- **Printed with 248 nm lithography**



Poly over STI



Metal 1

1.22 μm x 1.64 μm = 2.0 μm²

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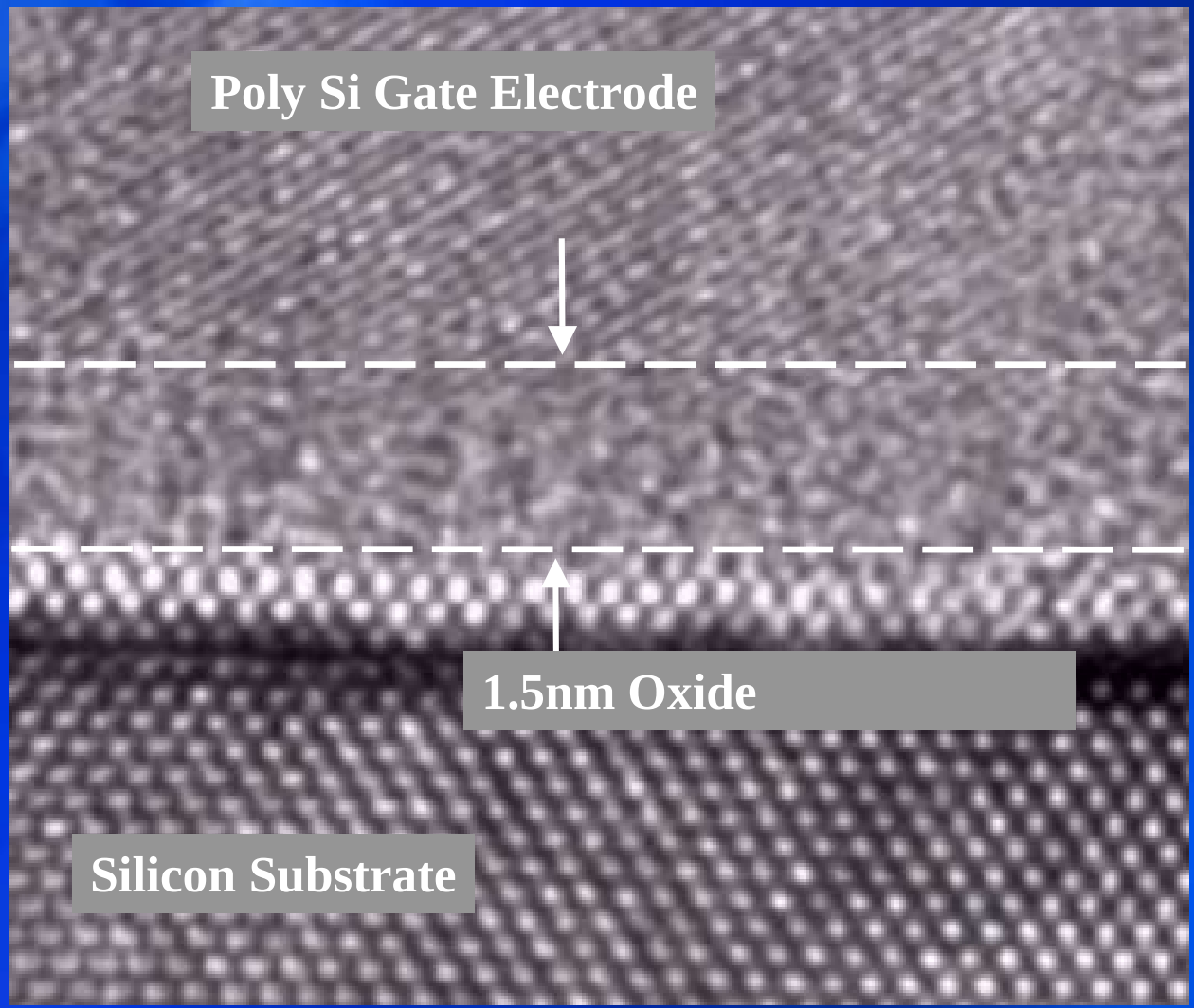
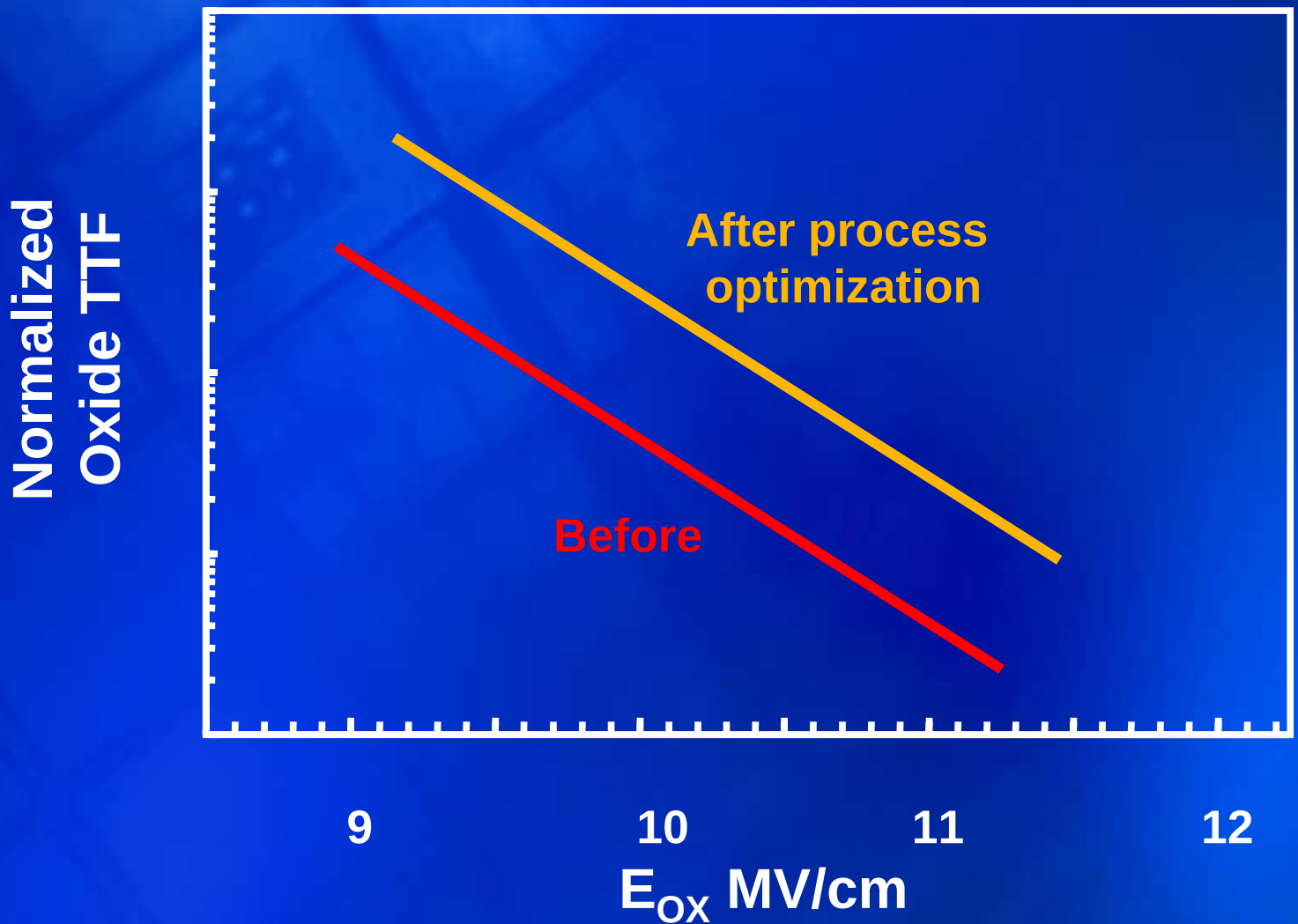
1.5nm Electrical T_{ox}



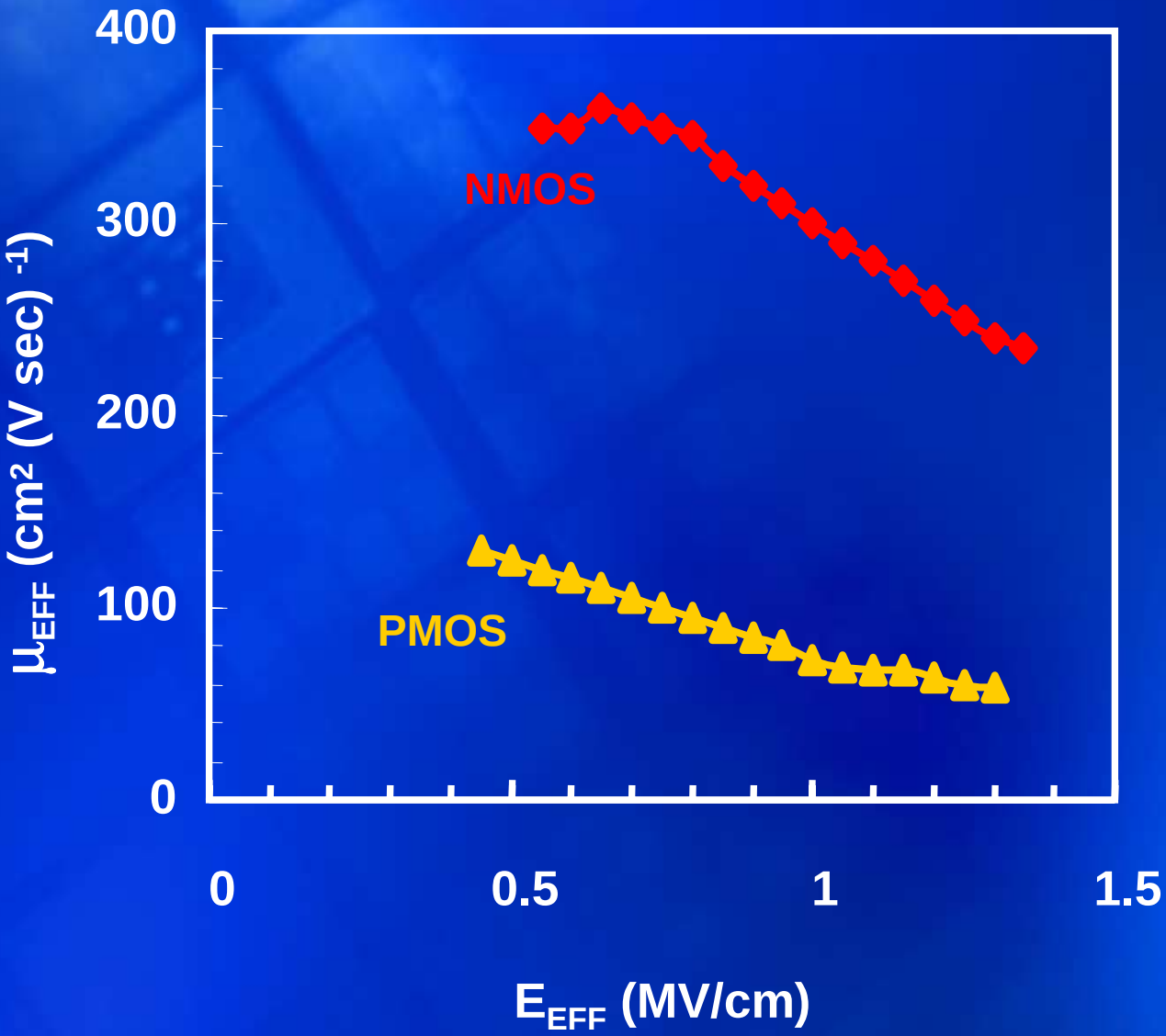
- Changes from Intel IEDM 2000 to support 10% higher E_{ox}

Improved Oxide Time to Fail



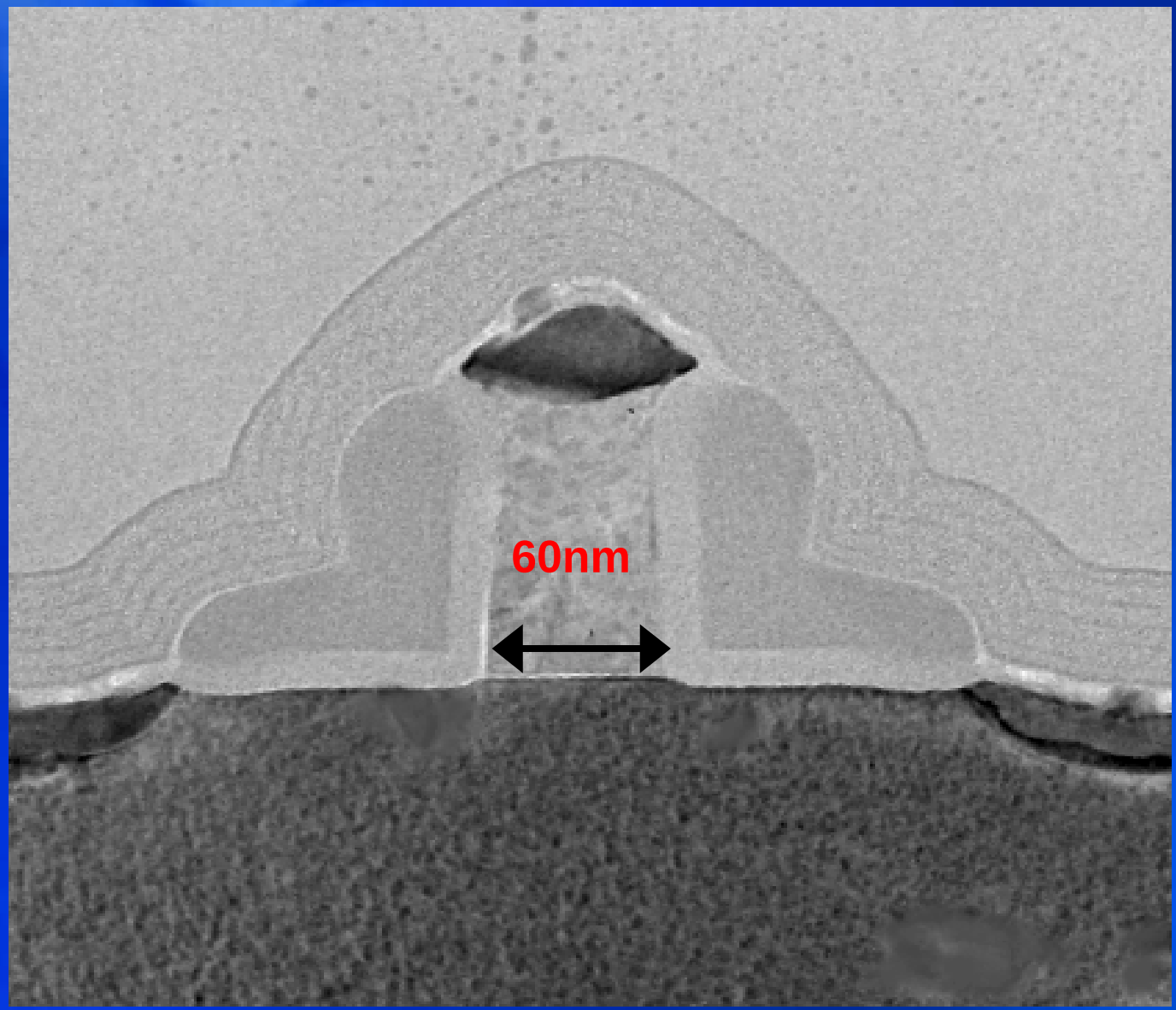
- **Same TTF: 10% higher oxide electric field**

High Channel Mobility



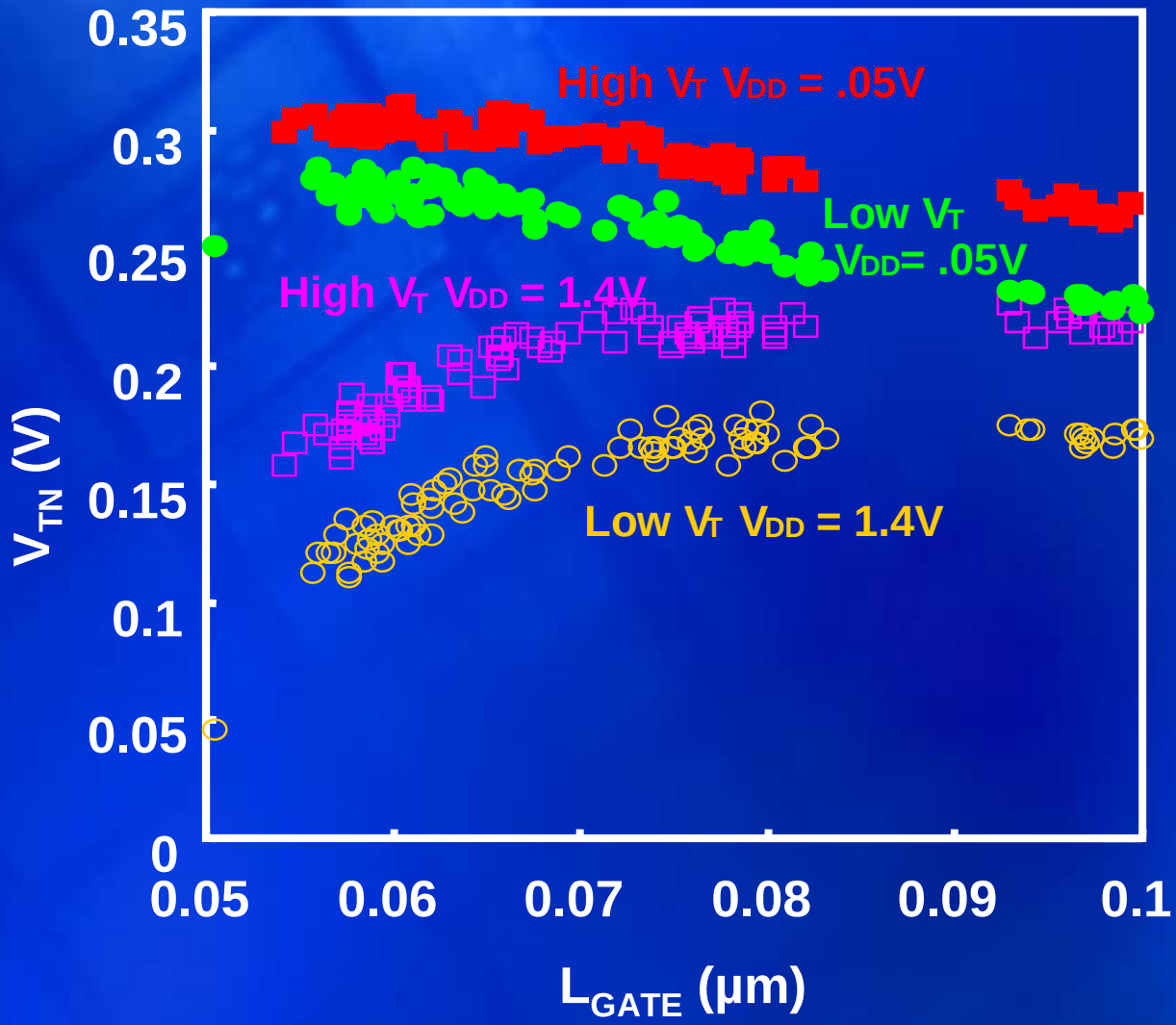
- Mobility improved over Intel IEDM 2000 for high drive current

60 nm Nominal Physical Gate Length



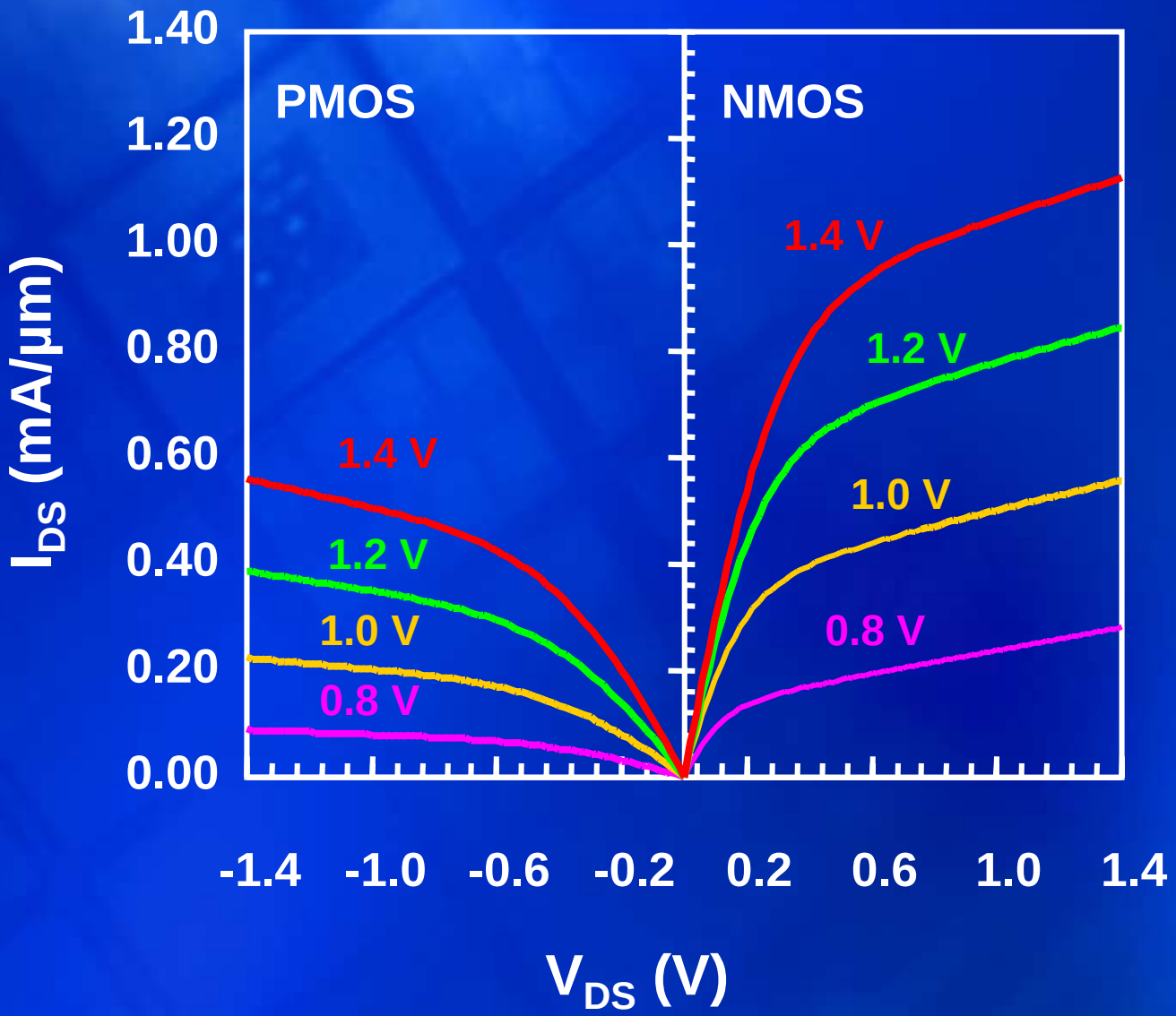
- Nominal L_{GATE} =60nm L_{MIN} = 60nm – CD control

Excellent Short Channel Effects (Low DIBL)



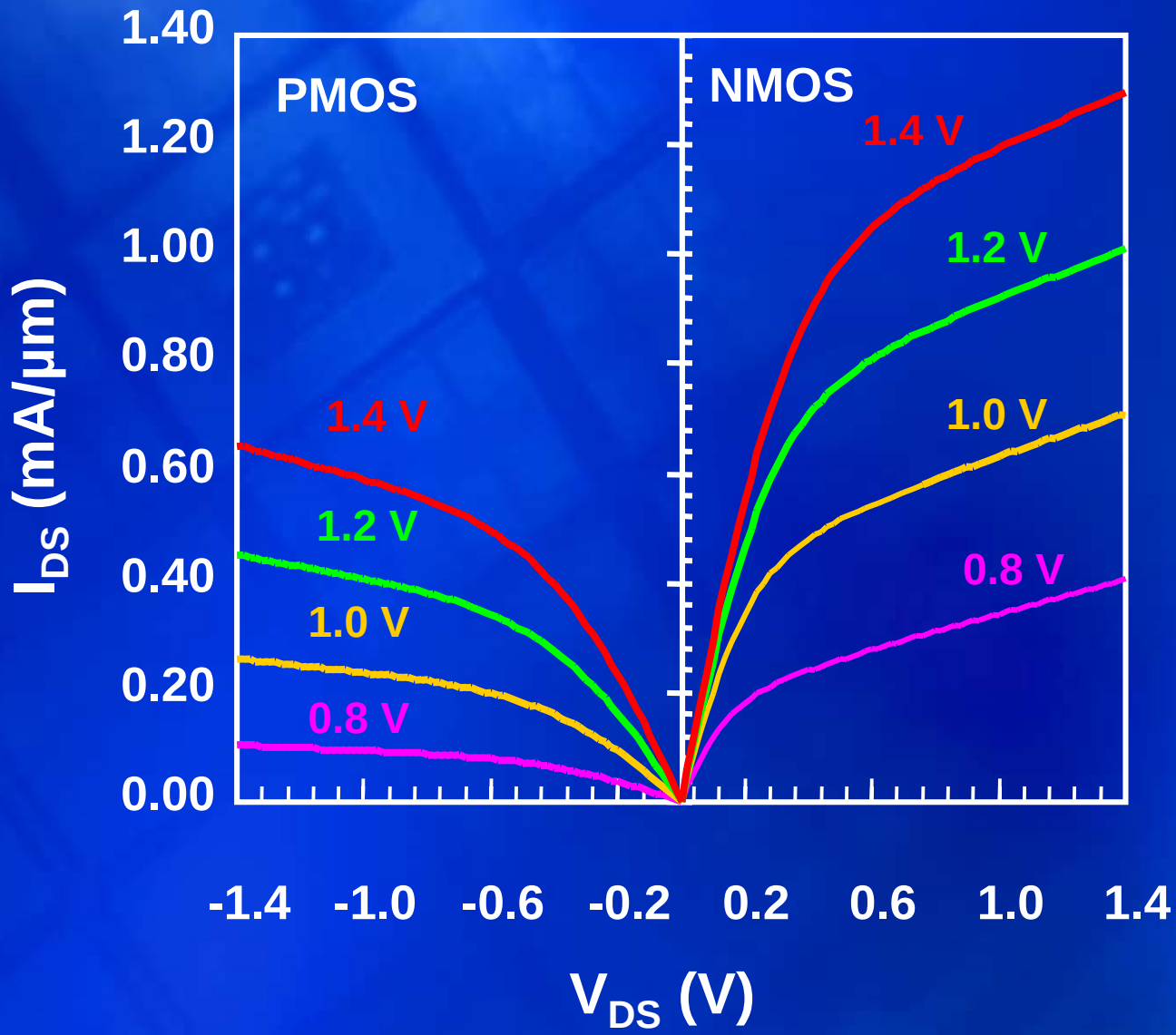
- Low DIBL < 100mV / V
- Key to high product performance

High V_T Device: I_D – V_D Curves



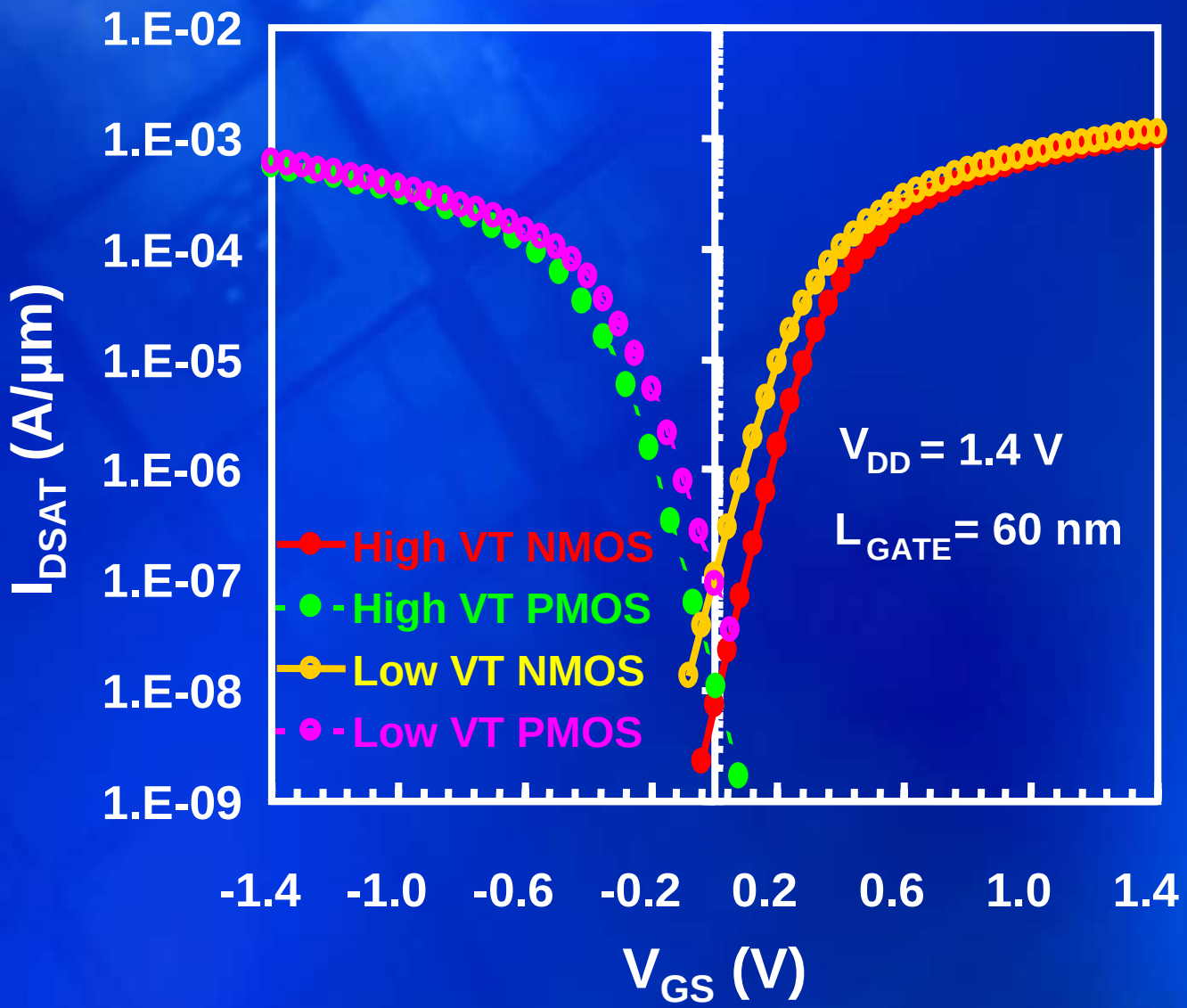
- 1.14 mA/μm NMOS
- 0.56 mA/μm PMOS

Low V_T Device: I_D – V_D Curves



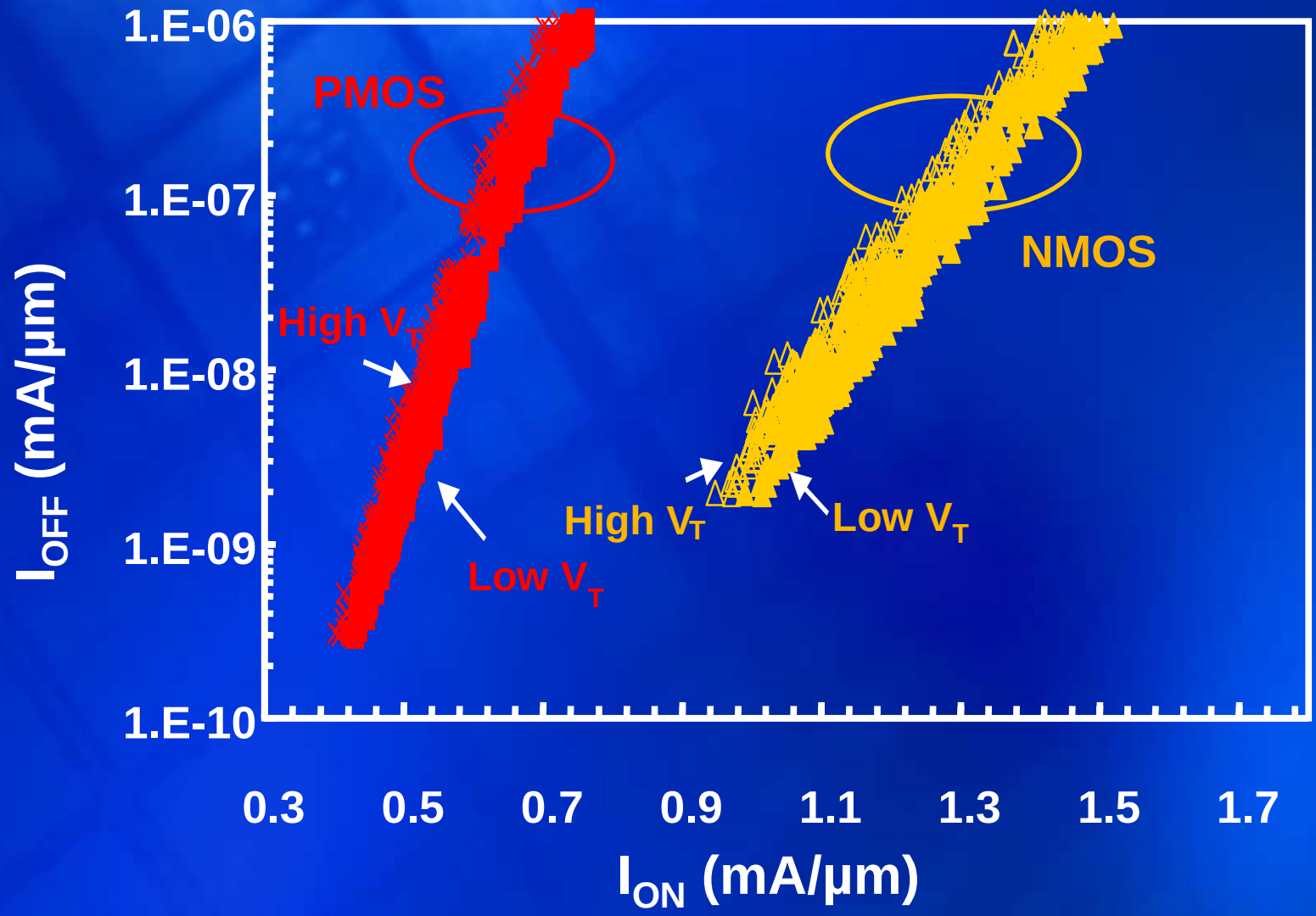
- Highest reported NMOS 1.30 mA/μm saturation current

Sub-Threshold Slope



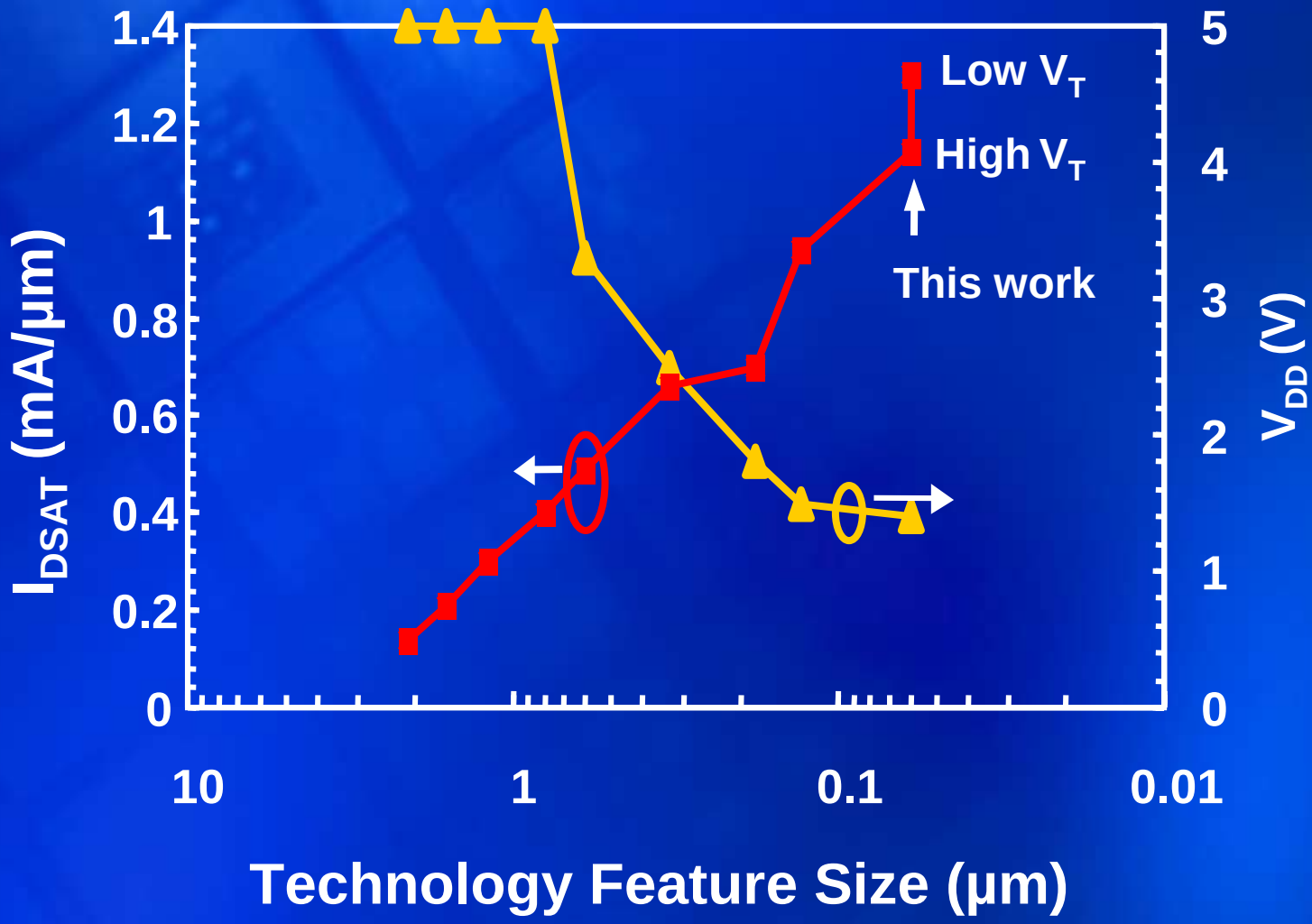
- Well controlled ~80mV sub-threshold slope

I_{ON} vs I_{OFF}



- Same I_{ON} vs I_{OFF} for low and high V_T devices

Intel NMOS Drive Current Trend



- Continues trend of higher drive current with each technology node

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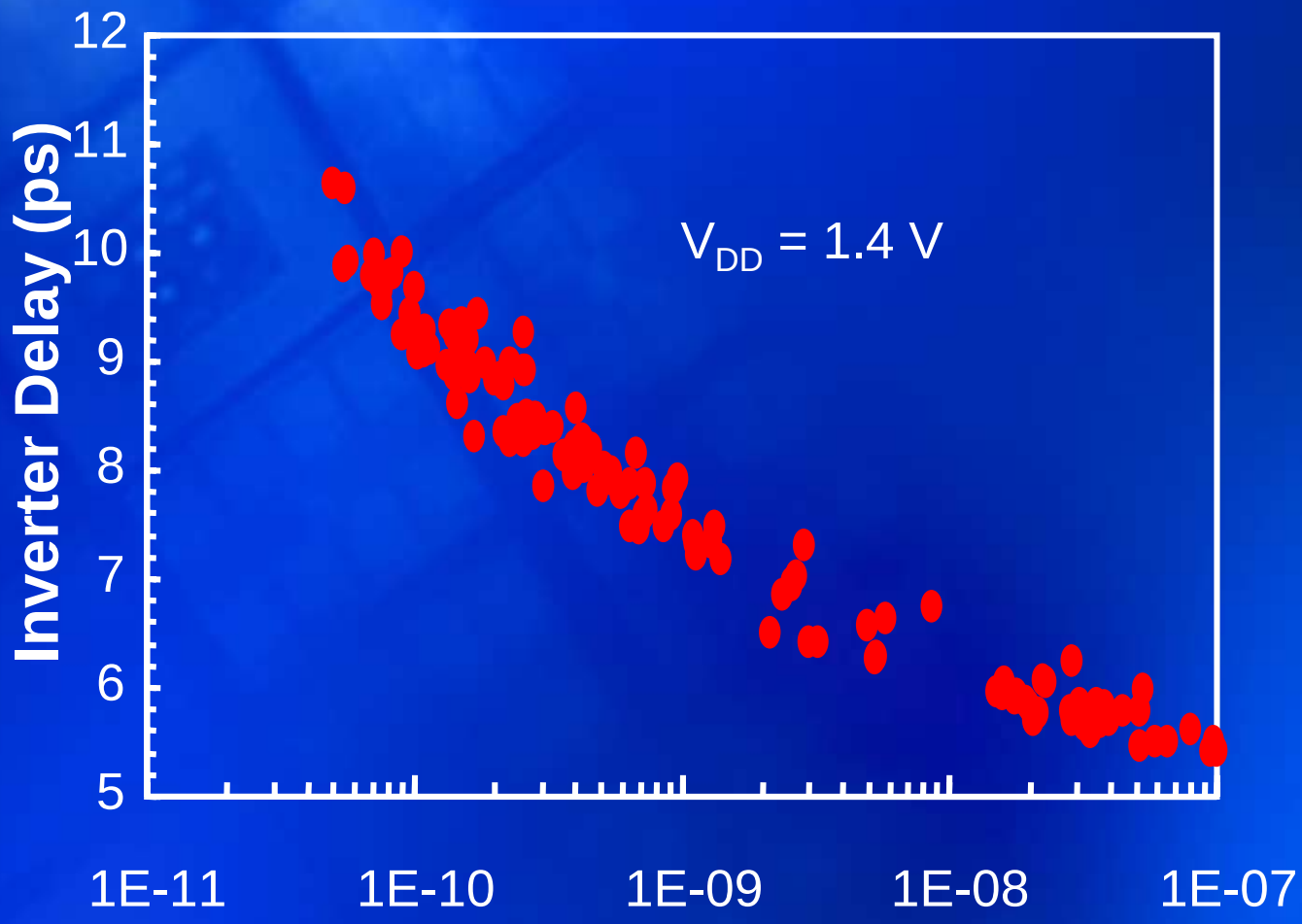
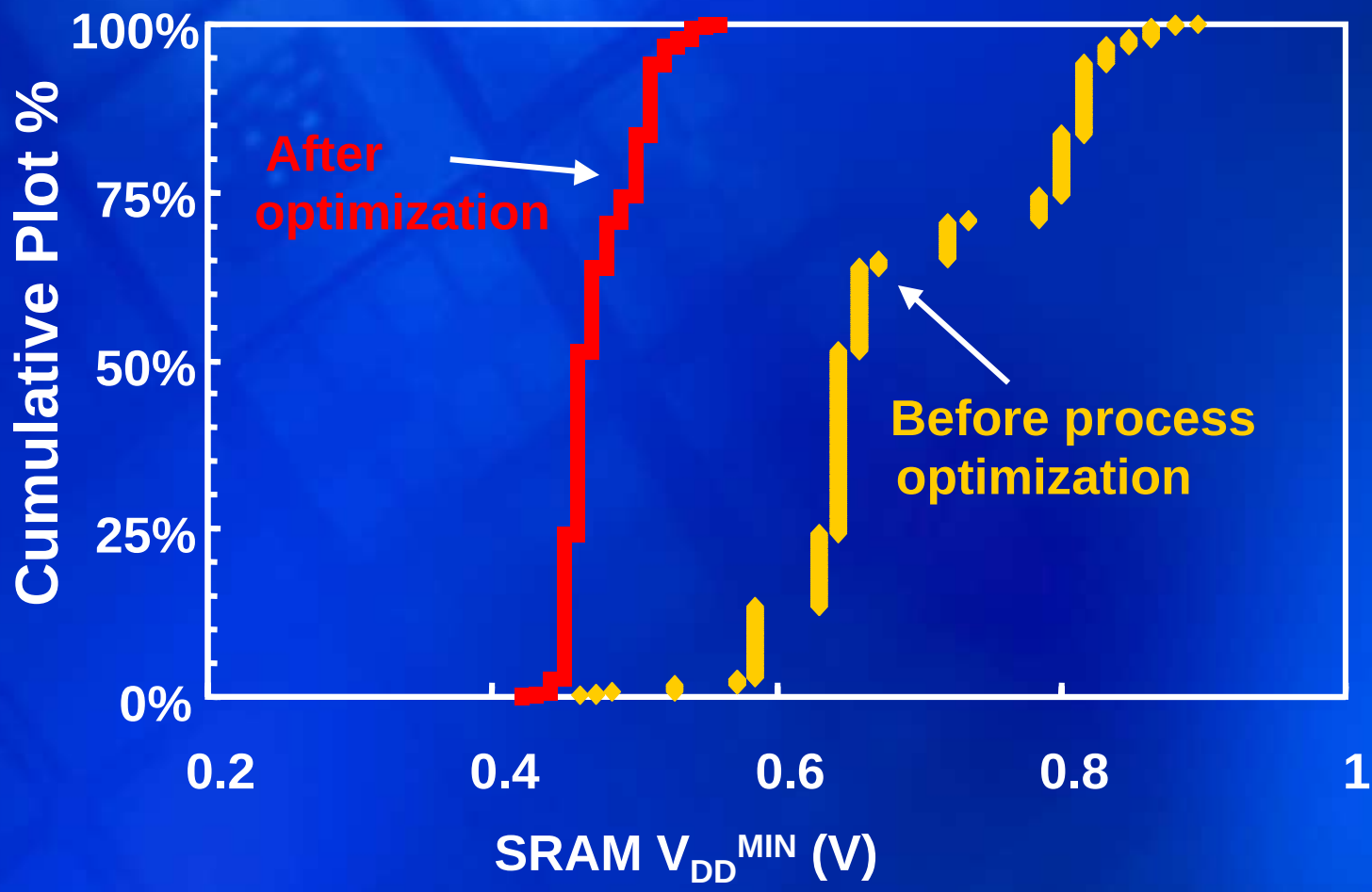
Inverter Delay

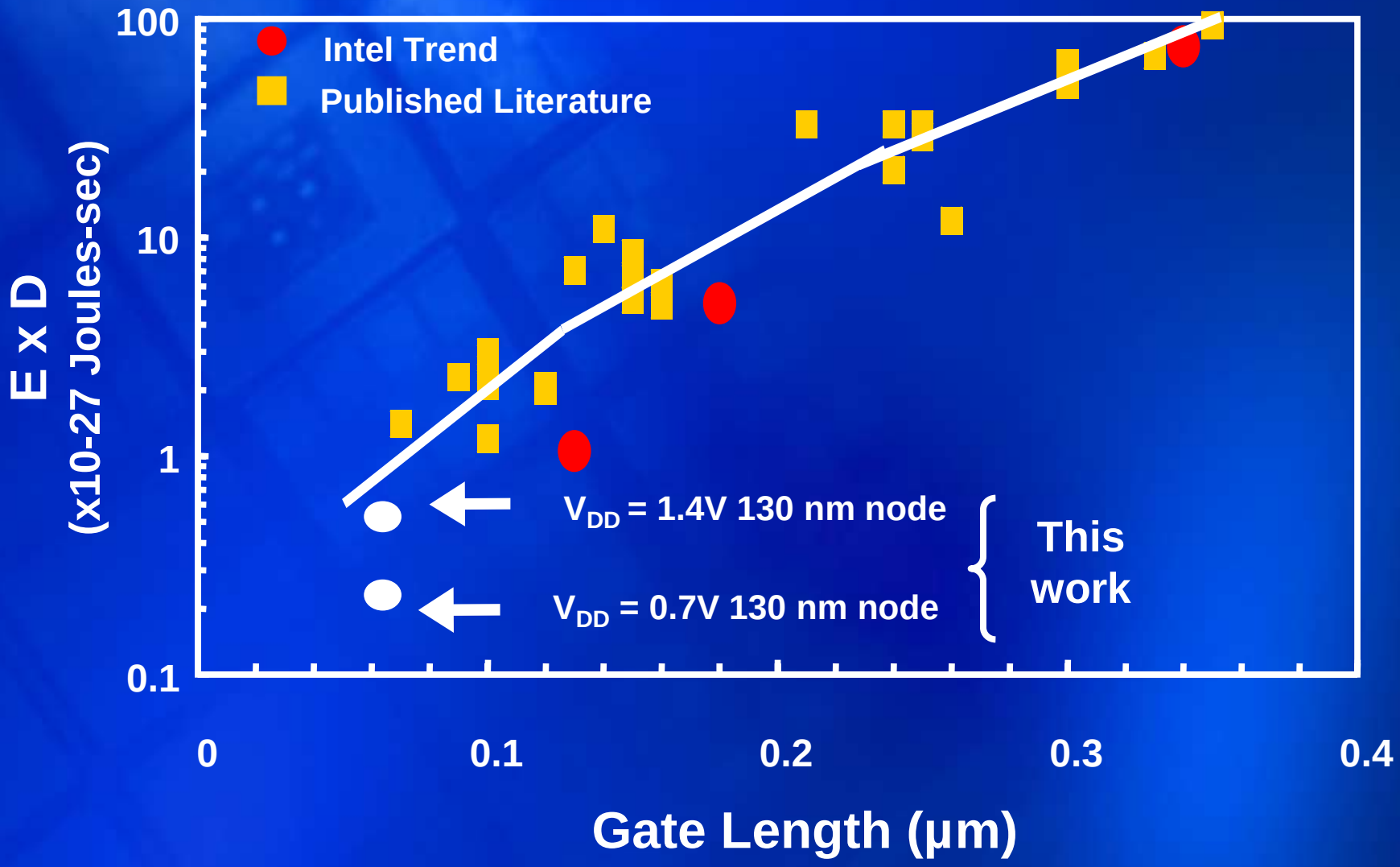


- **6.5 ps delay for I_{OFF} = 10 nA/μm**
- **5.5 ps delay for I_{OFF} = 100 nA/μm**

Low Voltage Operation

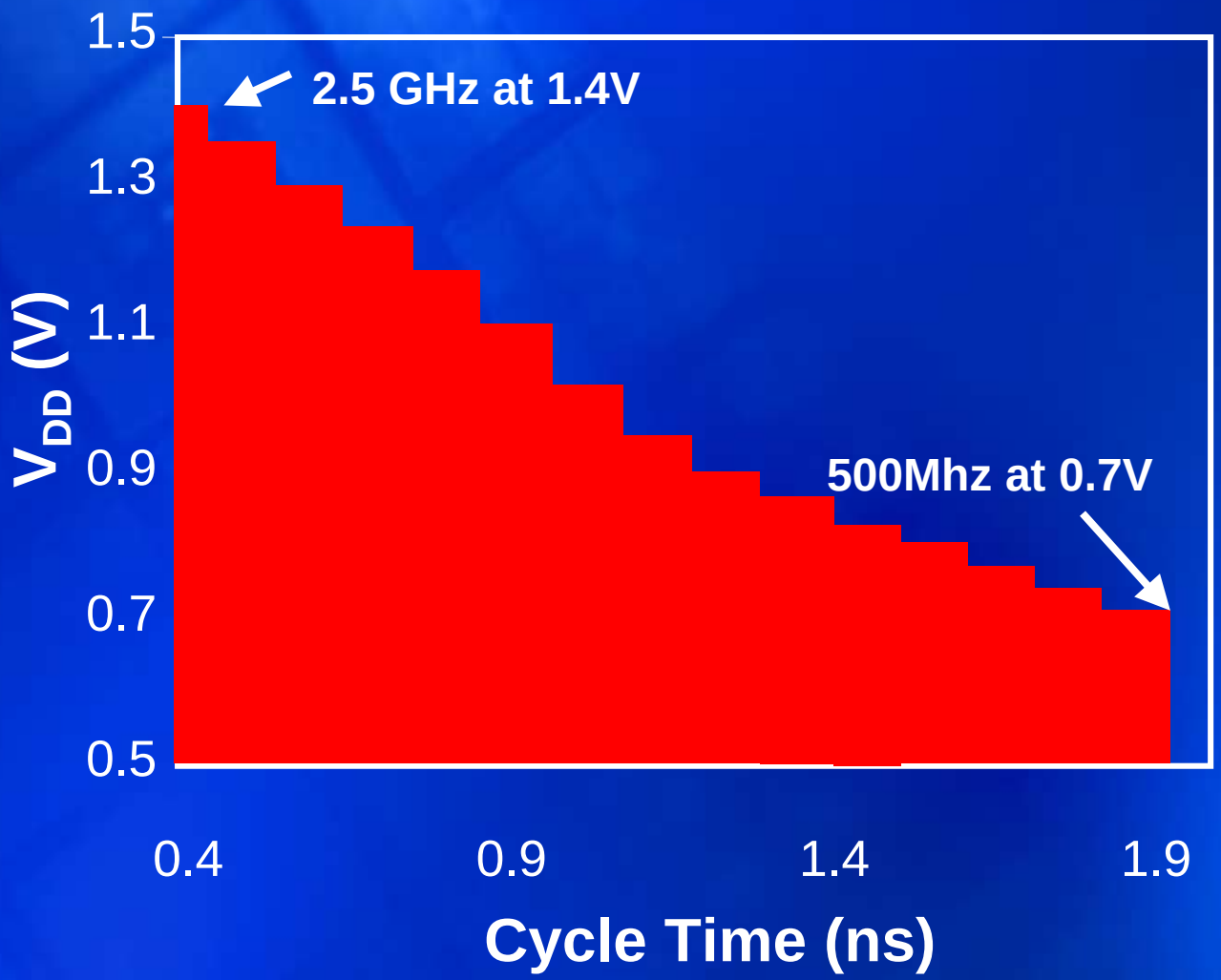


Leading Energy X Delay



- Industry leading energy delay product

Pentium® 4 Processors Schmoo Plot



- **Up to 2.5 Ghz operation**

Conclusions

- 60 nm transistors with NMOS drive current of 1.3 mA/μm achieved
- Low DIBL at < 100 mV / V
- Enhancements to process technology allows for 0.7 to 1.4 V operation
- Excellent integrated performance demonstrated
  - 5.5 to 6.5 ps inverter delay
  - 2.5 GHz operation

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